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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,456	08/30/2001	Gary L. Swoboda	TI-30478	9920

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EXAMINER	
GUILL, RUSSELL L	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,456	SWOBODA, GARY L.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/26/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 - 27 have been examined. Claims 1 - 27 have been rejected.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 5, 7, 10 - 11, 13 - 14, 17, 19, 22 - 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards065 (U.S. Patent 6,918,065) in view of Edwards047 (U.S. Patent 6,530,047).

3.1. Regarding claim 1, Edwards065 teaches:

3.1.1. A method of exporting from a data processor emulation information (**column 2, lines 9 - 15; and column 4, lines 5 - 15; and column 6, lines 1 - 15; and figure 1; and column 7, lines 45 - 50**) including emulation control information and emulation data (**figure 7; and Table 1; and Table 2; and Table 3; and Table 4**), comprising:

3.1.2. arranging the emulation information into information blocks (**figure 7; and Table 1; and Table 2; and Table 3; and Table 4**);

3.1.3. outputting a sequence of the information blocks from the data processor (**figure 8; and column 2, lines 10 - 67**); and

3.1.4. said arranging step including providing some of the information blocks of the sequence with relative proportions of emulation control information and emulation data that differ from the relative proportions of emulation control information and emulation data in other blocks of the sequence (**figure 8, elements 811, 812A, 812B, 813; and Table 1; and Table 2; and Table 3; and Table 4**).

3.2. Regarding claim 1, Edwards065 does not specifically teach:

3.2.1. outputting a sequence of the information blocks from the data processor ***via a plurality of terminals of the data processor***

3.3. Regarding claim 1, Edwards047 teaches:

3.3.1. outputting a sequence of the information blocks from the data processor via a plurality of terminals of the data processor (**figure 1, element 107; and figure 4; and figure 5; and column 7, lines 49 - 57**).

3.4. The motivation to use the art of Edwards047 with the art of Edwards065 would have been the benefit recited in Edwards047 that the widths of the link between the integrated circuit and the external system could be increased to meet debugging bandwidth needs of different applications (**column 7, lines 49 - 57**). Further, the same inventor produced both inventions. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Edwards047 with the art of Edwards065 to produce the claimed invention.

3.5. **Regarding claim 13**, Edwards065 teaches:

3.5.1. An integrated circuit device (**figure 1, element 101**), comprising:

3.5.2. a data processing portion for performing data processing operations (**figure 1, element 102**);

3.5.3. an emulation information collector coupled to said data processing portion for receiving emulation data therefrom (**figure 1, elements 102, 103, 104**), said collector operable for arranging the emulation data and associated emulation control information into information blocks (**figure 1, element 103; figure 7; and Table 1; and Table 2; and Table 3; and Table 4; and column 6, lines 1 - 15**);

3.5.4. a ***link*** coupled to said collector for permitting said collector to communicate with an ***external device*** located externally of said integrated circuit device (**figure 1, elements 103, 106, and unlabelled I/O link between elements 103 and 106; and column 6, lines 10 - 15**).

3.5.5. said collector operable for providing to said ***link*** a sequence of said information blocks to be output to the ***external device*** (**figure 7, figure 8, and column 6, lines 1 - 15**), said collector further operable for providing some of the information blocks of the sequence with relative proportions of emulation control information and emulation data that differ from the relative proportions of emulation control information and emulation data in other blocks of the sequence (**figure 8, elements 811, 812A, 812B, 813; and Table 1; and Table 2; and Table 3; and Table 4**).

3.6. **Regarding claim 13**, Edwards065 does not specifically teach:

3.6.1. ***a plurality of terminals coupled to said collector*** for permitting said collector to communicate with an emulation controller located externally of said integrated circuit device.

3.6.2. ***a plurality of terminals coupled to said collector*** coupled to said collector for permitting said collector to communicate with an ***emulation controller*** located externally of said integrated circuit device.

3.6.3. said collector operable for providing to said ***terminals*** a sequence of said information blocks to be output to the ***emulation controller***, said collector further operable for providing some of the information blocks of the sequence with relative proportions of emulation control information and emulation data that differ from the relative proportions of emulation control information and emulation data in other blocks of the sequence.

3.7. **Regarding claim 13**, Edwards047 teaches:

3.7.1. ***a plurality of terminals coupled to said collector*** for permitting said collector to communicate with an emulation controller located externally of said integrated circuit device **(figure 1, elements 107, 106, 103; and figure 4; and figure 5; and column 7, lines 49 - 57)**.

3.7.2. ***a plurality of terminals coupled to said collector*** coupled to said collector for permitting said collector to communicate with an ***emulation controller*** located externally of said integrated circuit device **(figure 1, elements 107, 106, 103; and figure 4; and figure 5; and column 7, lines 49 - 57; and column 8, lines 10 - 20)**.

3.7.3. said collector operable for providing to said ***terminals*** a sequence of said information blocks to be output to the ***emulation controller*** **(figure 1, elements 107, 106, 103; and figure 4; and figure 5; and column 7, lines 49 - 57; and column 8, lines 10 - 20)**.

3.8. The motivation to use the art of Edwards047 with the art of Edwards065 would have been the benefit recited in Edwards047 that the widths of the link between the integrated circuit and the external system could be increased to meet debugging bandwidth needs of different applications **(column 7, lines 49 - 57)**. Further motivation would have been the benefit recited in Edwards047 that the external system is capable of stopping, starting and resetting the processor through the link **(column 3, lines 14 - 20)**. Further, the same inventor produced both inventions. Therefore, as

discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Edwards047 with the art of Edwards065 to produce the claimed invention.

3.9. **Regarding claim 25**, Edwards065 teaches:

3.9.1. A data processing system (**figure 1**), comprising:

3.9.2. an integrated circuit (**figure 1, element 101**), including a data processing portion for performing data processing operations (**figure 1, element 102**);

3.9.3. an external device located externally of said integrated circuit and coupled to said integrated circuit (**figure 1, elements 103, 106, and unlabelled I/O link between elements 103 and 106**);

3.9.4. said integrated circuit including an emulation information collector coupled to said data processing portion for receiving emulation data therefrom (**figure 1, elements 102, 103, 104**), said collector operable for arranging the emulation data and associated emulation control information into information blocks (**figure 1, element 103; figure 7; and Table 1; and Table 2; and Table 3; and Table 4; and column 6, lines 1 - 15**); and

3.9.5. said collector coupled to said external device for permitting said collector to communicate with said external device (**figure 1, elements 103, 106, and unlabelled I/O link between elements 103 and 106; and column 6, lines 10 - 15**), said collector operable for outputting to said external device a sequence of said information blocks (**figure 7, figure 8, and column 6, lines 1 - 15**), said collector further operable for providing some of the information blocks with relative proportions of emulation control information and emulation data that differ from the relative proportions of emulation control information and emulation data in other blocks of the sequence (**figure 8, elements 811, 812A, 812B, 813; and Table 1; and Table 2; and Table 3; and Table 4**).

3.10. **Regarding claim 25**, Edwards065 does not specifically teach:

3.10.1. an ***emulation controller*** located externally of said integrated circuit and coupled to said integrated circuit ***for controlling emulation operations of said integrated circuit*** .

3.10.2. said collector coupled to said ***emulation controller*** for permitting said collector to communicate with said ***emulation controller***, said collector operable for outputting to said ***emulation controller*** a sequence of said information blocks, said collector further operable for providing some of the information blocks with relative proportions of emulation control information and emulation data that differ from the relative proportions of emulation control information and emulation data in other blocks of the sequence.

3.11. **Regarding claim 25**, Edwards047 teaches:

3.11.1. an ***emulation controller*** located externally of said integrated circuit and coupled to said integrated circuit ***for controlling emulation operations of said integrated circuit*** **(figure 1, elements 107, 106, 103; and figure 4; and figure 5; and column 7, lines 49 - 57; and column 8, lines 10 - 20).**

3.11.2. said collector coupled to said ***emulation controller*** for permitting said collector to communicate with said ***emulation controller***, said collector operable for outputting to said ***emulation controller*** a sequence of said information blocks **(figure 1, elements 107, 106, 103; and figure 4; and figure 5; and column 7, lines 49 - 57; and column 8, lines 10 - 20).**

3.12. The motivation would have been the same as claim 13 above. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Edwards047 with the art of Edwards065 to produce the claimed invention.

3.13. **Regarding claims 2 and 14**, Edwards 065 teaches:

3.13.1. That emulation control information in one of the information blocks includes information which identifies data in said one information block **(Table 1, fields "message type" and "source module").**

3.14. **Regarding claims 5 and 17**, Edwards 065 teaches:

3.14.1. That emulation data in one of the information blocks represents operations of a clock used by the data processor for performing data processing operations **(Table 1, field "Timestamp").**

3.15. **Regarding claims 7 and 19**, Edwards 065 teaches:

3.15.1. That each of the emulation blocks is a packet of emulation information including emulation control information **(figure 7, and Table 1).**

3.16. **Regarding claims 10 and 22**, Edwards 065 teaches:

3.16.1. That emulation control information in one of the information blocks indicates that the data processor has executed a program branch (**Table 5**).

3.17. **Regarding claims 11 and 23,** Edwards 065 teaches:

3.17.1. That emulation control information in one of the information blocks includes information about a memory access that has been executed by the data processor (**Table 2**).

4. Claims 3 - 4 and 15 - 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards065 (U.S. Patent 6,918,065) and Edwards047 (U.S. Patent 6,530,047), in view of Riley (U.S. Patent 5,832,490).

4.1. **Regarding claims 3 and 15,** Edwards065 teaches:

4.1.1. emulation control information (**figure 7; and Table 2**).

4.2. **Regarding claims 3 and 15,** Edwards065 does not specifically teach:

4.2.1. emulation control information ***in one of the information blocks includes information that identifies data in an information block other than said one information block***.

4.3. **Regarding claims 3 and 15,** Riley teaches:

4.3.1. control information in one of the information blocks includes information that identifies data in an information block other than said one information block (**figure 2; and column 4, lines 20 - 50**).

4.4. **Regarding claims 4 and 16,** Edwards065 teaches:

4.4.1. emulation control information (**figure 7; and Table 2**).

4.5. **Regarding claims 4 and 16,** Edwards065 does not specifically teach:

4.5.1. emulation control information ***in one of the information blocks includes a compression map***.

4.6. **Regarding claims 4 and 16,** Riley teaches:

4.6.1. control information in one of the information blocks includes a compression map (**figure 2; and column 4, lines 20 - 50**).

4.7. The motivation to use the art of Riley with the art of Edwards065 would have been the benefit of solutions provided for methods of preparing and sending packets of compressed data **(figure 2; and column 4, lines 20 - 50)**. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Riley with the art of Edwards065 to produce the claimed inventions.

5. Claims 6, 8, 9, 12, 18, 20, 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards065 (U.S. Patent 6,918,065) and Edwards047 (U.S. Patent 6,530,047), in view of Tanenbaum (Tanenbaum, Andrew S.; "Computer Networks", 1996, Third Edition, Prentice-Hall).

5.1. **Regarding claim 6 and 18,** Edwards065 teaches:

5.1.1. emulation control information and emulation data in blocks **(figure 7; and Table 2)**.

5.2. **Regarding claim 6 and 18,** Edwards065 does not specifically teach:

5.2.1. The relative proportions of ***emulation control information and emulation data*** in said some ***blocks*** are respectively 100% and 0%.

5.3. **Regarding claim 6 and 18,** Tanenbaum teaches:

5.3.1. The relative proportions of control information and data in the blocks are respectively 100% and 0% **(page 227, figure 3-25 (b))**.

5.4. **Regarding claim 8 and 20,** Edwards065 teaches:

5.4.1. Emulation control information **(figure 7; and Table 2)**.

5.5. **Regarding claim 8 and 20,** Edwards065 does not specifically teach:

5.5.1. Emulation control information ***in one of the information blocks includes a unique identifier which indicates that the corresponding data in said one information block is a portion of a larger unit of data which has another portion in another information block of the sequence***.

5.6. **Regarding claim 8 and 20,** Tanenbaum teaches:

5.6.1. information in one of the information blocks includes a unique identifier which indicates that the corresponding data in said one information block is a portion of a larger unit of data

which has another portion in another information block of the sequence (**pages 406 - 407, section 5.4.6 Fragmentation; and page 409, text and figure 5-42**).

5.7. **Regarding claim 9 and 21**, Edwards065 does not specifically teach:

5.7.1. Another information block is an earlier block in the sequence.

5.8. **Regarding claim 9 and 21**, Tanenbaum teaches:

5.8.1. Another information block is an earlier block in the sequence (**pages 406 - 407, section 5.4.6 Fragmentation; and page 409, text and figure 5-42**).

5.9. **Regarding claim 12 and 24**, Edwards065 teaches:

5.9.1. Emulation control information (**figure 7; and Table 2**).

5.10. **Regarding claim 12 and 24**, Edwards065 does not specifically teach:

5.10.1. Emulation control information ***in one information block of the sequence affects how*** emulation control information ***in another information block of the sequence is to be interpreted.***

5.11. **Regarding claim 12 and 24**, Tanenbaum teaches:

5.11.1. control information in one information block of the sequence affects how control information in another information block of the sequence is to be interpreted (**pages 406 - 407, section 5.4.6 Fragmentation; and page 409, text and figure 5-42**).

5.12. The motivation to use the art of Tanenbaum with the art of Edwards065 would have been the benefit of solutions provided for methods of transmitting packets of data (**page 227, pages 406 - 409**). Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Tanenbaum with the art of Edwards065 to produce the claimed inventions.

6. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards065 (U.S. Patent 6,918,065) and Edwards047 (U.S. Patent 6,530,047), in view of Miyayama (U.S. Patent 6,665,821).

6.1. **Regarding claim 26,** Miyayama teaches: a man/machine interface coupled to aid emulation controller for permitting a user to communicate with said emulation controller **(figure 1, element "Host System")**.

6.2. **Regarding claim 27,** Miyayama teaches: the man/machine interface is a visual interface **(figure 1, element "Host System")**.

6.3. The motivation to use the art of Miyayama with the art of Edwards065 would have been the benefit recited in Miyayama that the debbuging tool can provide perform various processes necessary for debugging **(column 1, lines 20 - 30)**. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Miyayama with the art of Edwards065 to produce the claimed invention.

Conclusion

7. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

    7.1.1. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure:

        7.1.1.1. Stence (Stence, Ronald; "A New Development Tool Standard with the IEEE-ISTO", 1999, International Conference on Computer Design, 10-13 Oct. 1999

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.
10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

Paul L. Rodriguez 7/15/05

Primary Examiner
Art Unit 2125